

The diagram illustrates the internal architecture of a video controller 510. It features several key components and signal paths:

- Input and Initial Processing:** Incoming data (516) enters from the bottom right. It is processed by an **EVENT/ODD ACTIVE** block (519) and a **CLOCK** input. These signals are combined in an **AND** gate (517) to produce a **DISPLAY ENABLE** signal (518).
- Register and Multiplexer Stage:** The **DISPLAY ENABLE** signal (518) is fed into an **EVEN REGISTER** (512) and an **ODD REGISTER** (511). The outputs of these registers are combined in a **MUX** (520).
- Processing Blocks:** The output of the MUX (520) is sent to the **LSFR** (532) block. This block is part of a larger processing unit that also includes a **BLOCK MODULE** (534), an **OUTPUT FUNCTION** (536), and an **HD CP CIPHER** (530).
- Clock and Data Splitting:** A **330 MHz CLOCK** (513) is distributed to the LSFR (532), the MUX (520), and a **1/2 CLOCK** block (542). The 1/2 CLOCK (542) also provides a **165 MHz CLOCK** (514) to the **DATA SPLITTER** (540).
- Data Splitting and Output:** The **DATA SPLITTER** (540) takes data from the processing unit and splits it into **EVEN** and **ODD** channels (labeled C and D). These channels are then sent to the **DVO PORT** (546) for output to the external display (E).

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